1uA I_Q, 250mA CMOS Linear Regulator

General Description

The EMP8150 features of low quiescent current as low as 1uA and almost zero disable current is ideal for powering the battery equipment to a longer service life. It guarantees delivery of 250mA output current and supports preset output voltages ranging from 0.8V to 4.0V with 0.1V increment. The regulator is stable with small ceramic capacitive loads.

The EMP8150 is available in miniature uDFN-4, SOT-23-5 and SOT-23-3 packages.

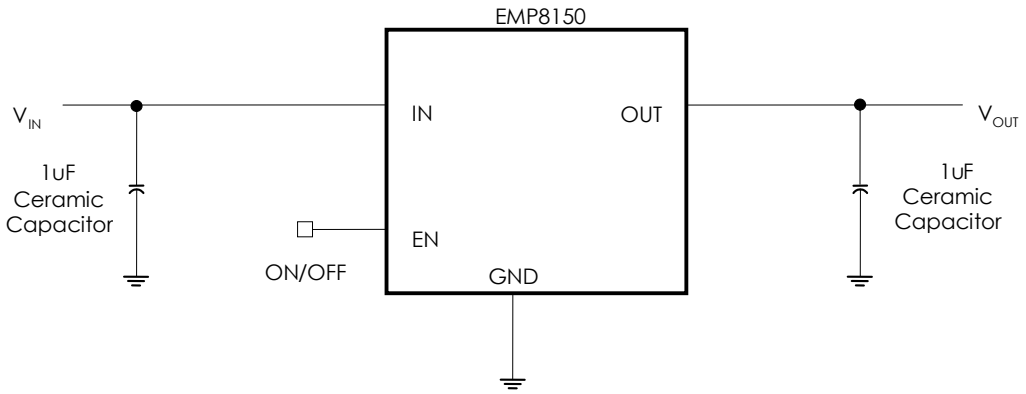
Applications

- Portable information appliances
- Battery-powered systems
- Ultra Low Power Applications

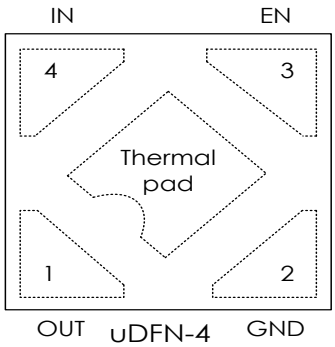
Features

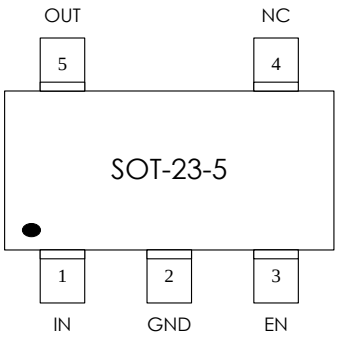
- 1μA typical quiescent current at no Load
- 1.8V to 5.5V input range
- ±1% output voltage tolerance
- 250mA guaranteed output current
- 150mV (V_{OUT}=3.3V) typical dropout at 250mA
- Less than 0.1μA typical shutdown current
- 250mA(V_{IN}≧2.4V) output current with EN
- Auto-discharge during chip disable
- 0.8V to 4.0V output voltage range
- Stable with small ceramic output capacitors
- Fold-back over current protection
- Over Temperature Protection

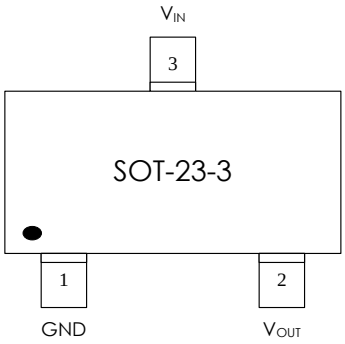
Typical Application



Connection Diagrams







Order information

EMP8150-XXFJ04NRR

XX	Output voltage
FJ04	uDFN-4 Package
NRR	RoHS & Halogen free package Rating: -40 to 85°C Package in Tape & Reel

EMP8150-XXVN05NRR

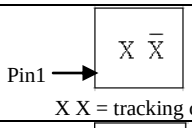
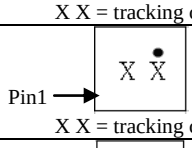
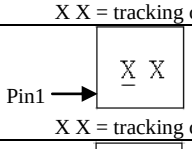
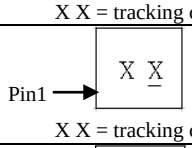
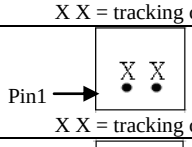
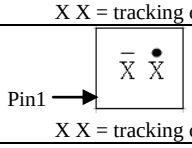
XX	Output voltage
VN05	SOT-23-5 Package
NRR	RoHS & Halogen free package Rating: -40 to 85°C Package in Tape & Reel

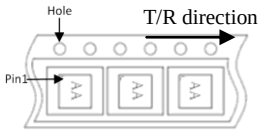
EMP8150-XXVN03NRR

XX	Output voltage
VN03	SOT-23-3 Package
NRR	RoHS & Halogen free package Rating: -40 to 85°C Package in Tape & Reel

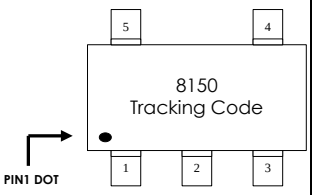
Order, Marking & Packing Information

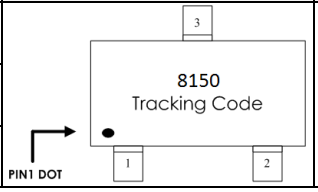
Package	Vout	Product ID.	Marking	Packing
uDFN-4	3.3V	EMP8150-33FJ04NRR	Pin1 → X X X X = tracking code	Tape & Reel 8Kpcs
	3.1V	EMP8150-31FJ04NRR	Pin1 → X X X X = tracking code	
	3.0V	EMP8150-30FJ04NRR	Pin1 → X X X X = tracking code	

	2.8V	EMP8150-28FJ04NRR		
	2.2V	EMP8150-22FJ04NRR		
	1.8V	EMP8150-18FJ04NRR		
	1.5V	EMP8150-15FJ04NRR		
	1.25V	EMP8150-1CFJ04NRR		
	1.2V	EMP8150-12FJ04NRR		



Note : When the hole is located above the tape, the pin1 of the IC is located on the upper left.

Package	Vout	Product ID.	Marking	Packing
SOT-23-5	3.3V	EMP8150-33VN05NRR		Tape & Reel 3Kpcs
	3.1V	EMP8150-31VN05NRR		
	3.0V	EMP8150-30VN05NRR		
	2.8V	EMP8150-28VN05NRR		
	1.9V	EMP8150-19VN05NRR		
	1.8V	EMP8150-18VN05NRR		
	1.5V	EMP8150-15VN05NRR		
	1.25V	EMP8150-1CVN05NRR		
	1.2V	EMP8150-12VN05NRR		
	0.8V	EMP8150-08VN05NRR		

Package	Vout	Product ID.	Marking	Packing
SOT-23-3	3.3V	EMP8150-33VN03NRR		Tape & Reel 3Kpcs
	3.0V	EMP8150-30VN03NRR		
	2.8V	EMP8150-28VN03NRR		

	1.9V	EMP8150-19VN03NRR		
	1.8V	EMP8150-18VN03NRR		
	1.5V	EMP8150-15VN03NRR		
	1.2V	EMP8150-12VN03NRR		

Pin Functions

Name	uDFN-4	SOT-23-5	SOT-23-3	Function
IN	**4**	**1**	**3**	**Supply Voltage Input.** Require a minimum input capacitor of close to 1μF ceramic capacitor to ensure stability and sufficient decoupling from the ground pin.
GND	**2**	**2**	**1**	**Ground Pin.**
EN	**3**	**3**	**N/A**	**Enable Input.** Enable the regulator by pulling the EN pin High. To keep the regulator on during normal operation, connect the EN pin to V_{IN}. The EN pin must not exceed V_{IN} under all operating conditions.
NC	**N/A**	**4**	**N/A**	**No Connected.**
OUT	**1**	**5**	**2**	**Regulated Output Voltage Pin.** A small 1μF ceramic capacitor is needed from this pin to ground to assure stability.
Thermal Pad	**YES**	**N/A**	**N/A**	The thermal pad with large thermal land area on the PCB will helpful chip power dissipation, to connect it to GND together normally.

Functional Block Diagram

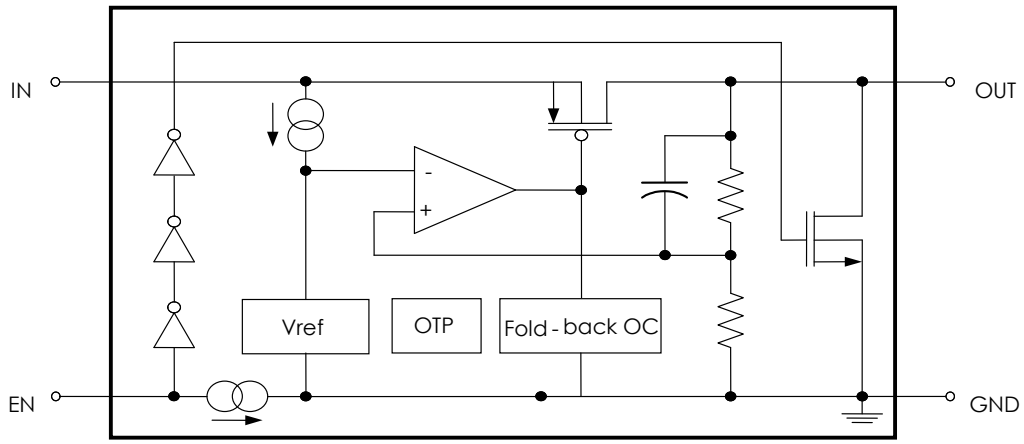


FIG.1. Functional Block Diagram of EMP8150

Absolute Maximum Ratings (Notes 1, 2)

IN, EN, OUT	-0.3V to 6.5V	ESD Rating	
Power Dissipation	(Note 6)	Human Body Model	2KV
Storage Temperature Range	-65°C to 150°C	Charged device Model	750V
Junction Temperature (T_J)	150°C	Latch-up	200mA
Lead Temperature (Soldering, 10 sec.)	260°C		

Operating Ratings (Note 1, 2)

Supply Voltage	Vout+1V to 5.5V	Operating Temperature Range	-40°C to 85°C
		Junction Temperature (T_J)	-40°C to 125°C

Thermal Resistance:

Symbol	θ_{JA}(Note 3)	θ_{JC}(Note 4)
uDFN-4	110(℃/W)	23(℃/W)
SOT-23-5	152(℃/W)	81(℃/W)
SOT-23-3	250(℃/W)	81(℃/W)

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V_{IN} = V_{OUT} +1V (Note 5), V_{EN}=V_{IN}, C_{IN} = 1uF, C_{OUT} =1uF, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ (Note 7)	Max	Units
V_{IN}	Input Voltage	I_{OUT} = 150mA	1.8		5.5	V
		I_{OUT} = 250mA	2.4		5.5	
V_{OUT}	Output Voltage		0.8		3.3	V
Δ V_{OTL}	Output Voltage Tolerance	Vout>2.0V, T=25	X0.99		X1.01	V
		Vout<=2.0V, T=25	-20		+20	mV
I_{OUT}	Maximum Output Current	Average DC Current Rating	250			mA
I_{cl}	Current Limit			400		mA
I_{SC}	Short Current Limit			180		mA
T_{SD}	Thermal Shutdown			160		℃
	Thermal Shutdown Hysteresis			20		
I_Q	Quiescent Current	I_{OUT} = 0mA		1	2	μA
I_{EN}	Shutdown Supply Current	V_{OUT} = 0V, EN = GND		0.1	0.5	μA
V_{DO}	Dropout Voltage (Note 5)	I_{OUT} = 250mA, Vout=0.8V		1020	2000	mV
		I_{OUT} = 250mA, Vout=1.2V		825	1600	
		I_{OUT} = 250mA, Vout=1.5V		435	870	
		I_{OUT} = 250mA, Vout=1.8V		275	555	
		I_{OUT} = 250mA, Vout=2.8V		155	315	
		I_{OUT} = 250mA, Vout=3.3V		150	300	
Δ V_{OUT}	Line Regulation	I_{OUT} = 1mA, (V_{OUT} + 1V) ≤ V_{IN} ≤ 5.5V		0.02	0.1	%/V
	Load Regulation	1mA ≤ I_{OUT} ≤ 250mA		10	30	mV
PSRR	Power supply rejection ratio	f = 1kHz, Ripple 0.2 Vp-p, V_{IN}=2.4V, Iout = 30mA, Vout=0.8V		75		dB
e_n	Output Voltage Noise	10Hz ≤ f ≤ 100kHz V_{IN}=2.4V, Iout = 30mA, Vout=0.8V		60		μV_{RMS}
V_{EN}	EN Input Threshold		1.2			V
					0.4	
I_{EN}	EN Input Bias Current	EN=GND or V_{IN}		0.1	1	μA

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

Note 3: θ_{JA} is measured in the natural convection at T_A=25℃ on a high effective thermal conductivity test board (2 layers, 2S0P).

Note 4: θ_{JC} represents the resistance to the heat flows the chip to package top case.

Note 5: Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at $V_{IN} - V_{OUT}$ = 1V.

Note 6: Maximum Power dissipation for the device is calculated using the following equations:

$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

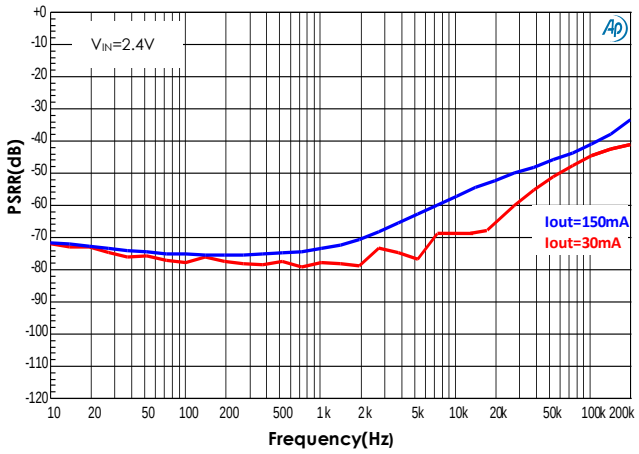
Where T_J(MAX) is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. E.g. for the uDFN-4 packageθ_{JA} = 110°C/W, T_J (MAX) = 150°C and using T_A = 25°C, the maximum power dissipation is found to be 1.13W. The derating factor (-1/θ_{JA}) = -9.1mW/°C, thus below 25°C the power dissipation figure can be increased by 6.6mW per degree, and similarity decreased by this factor for temperatures above 25°C.

Note 7: Typical values represent the most likely parametric norm.

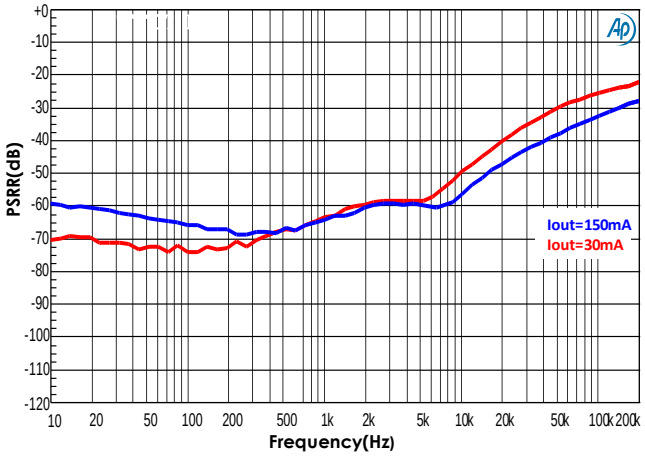
Typical Performance Characteristics

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} =1uF, C_{OUT} =1uF, T_A = 25°C

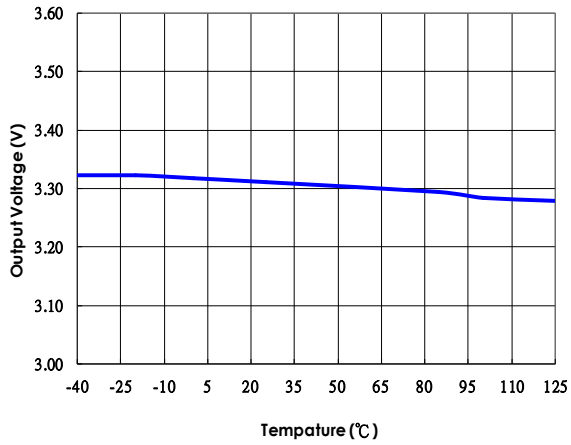
PSRR vs. Frequency (V_{OUT}=0.8V)



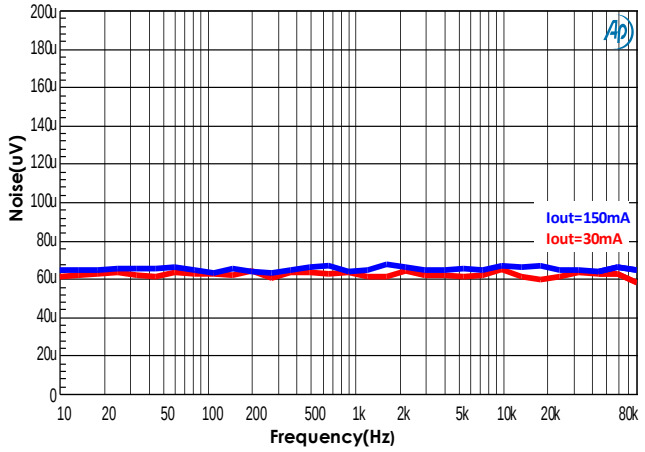
PSRR vs. Frequency (V_{OUT}=3.3V)



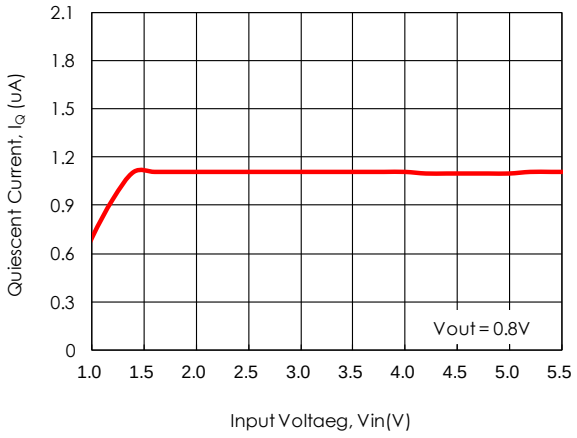
Output Voltage vs. Temperature



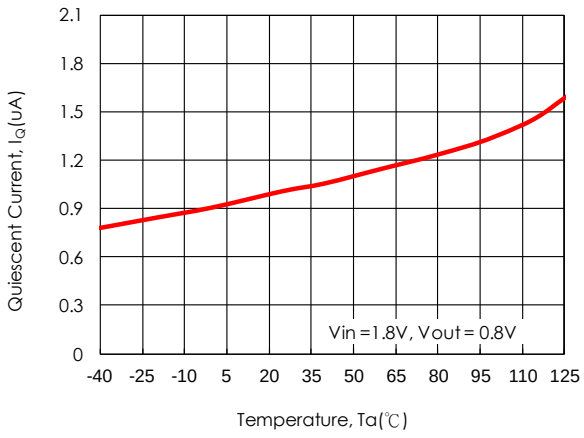
Output Voltage Noise (V_{OUT}=3.3V)



Quiescent Current vs. Input Voltage



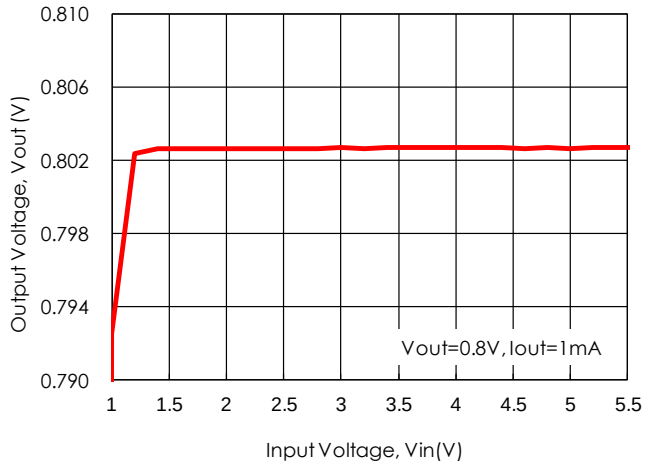
Quiescent Current vs. Temperature



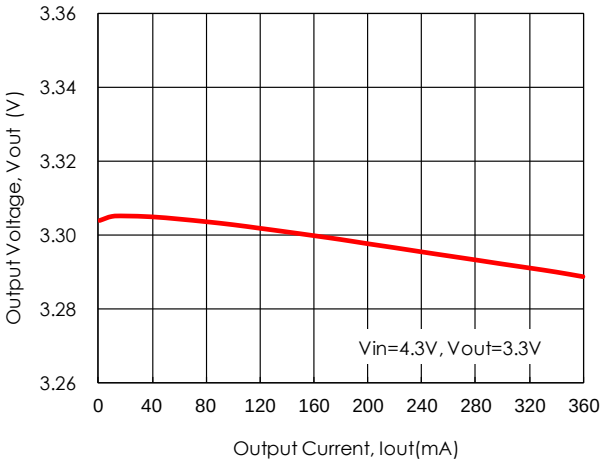
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} =1uF, C_{OUT} =1uF, T_A = 25°C

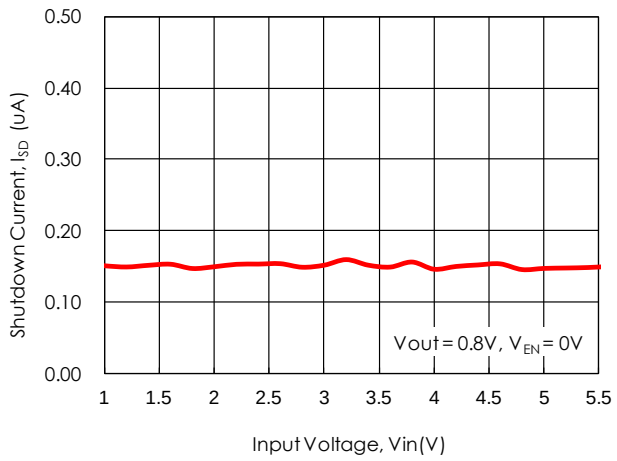
Output Voltage vs. Input Voltage (V_{OUT}=0.8V)



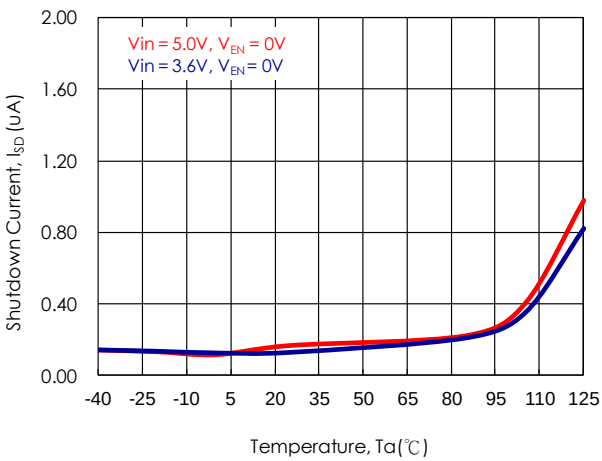
Output Voltage vs. Output Current (V_{OUT}=3.3V)



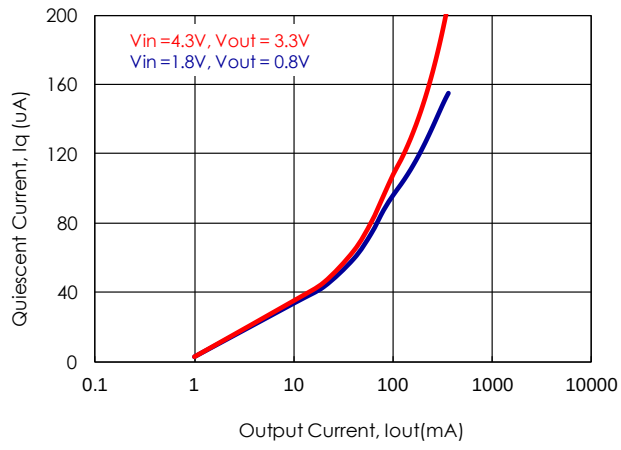
Shutdown Current vs. Input Voltage



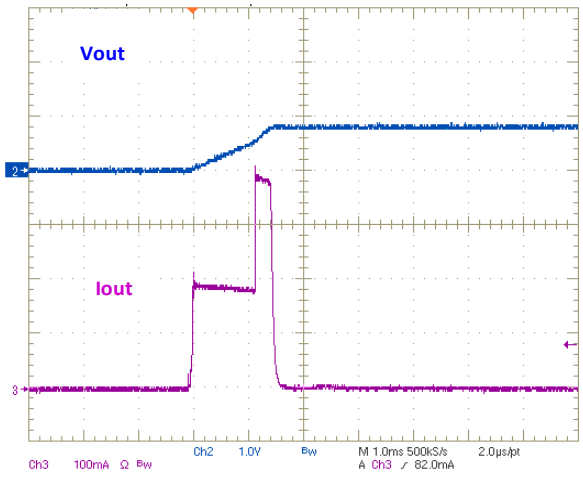
Shutdown Current vs. Temperature



Quiescent Current vs. Output Current



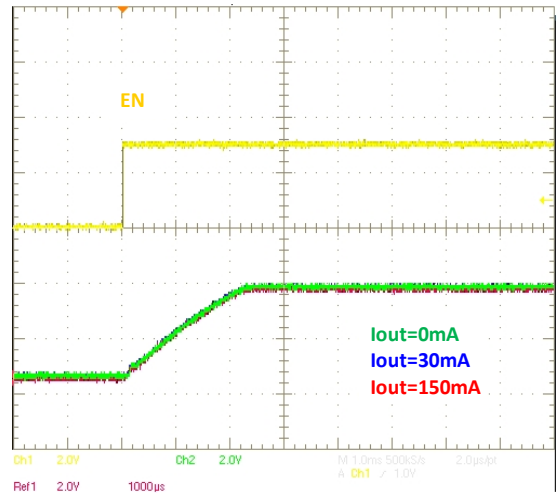
Output Current Limit (Fold-back,V_{OUT}=0.8V)



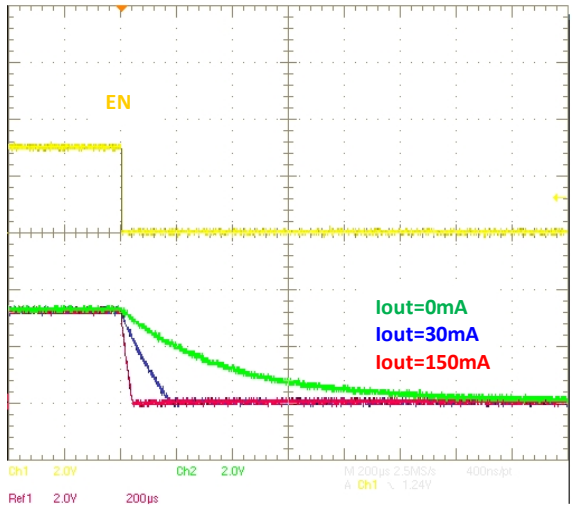
Typical Performance Characteristics (cont.)

Unless otherwise specified, V_{IN} = $V_{OUT\ (NOM)}$ + 1V, V_{EN}=V_{IN}, C_{IN} =1uF, C_{OUT} =1uF, T_A = 25°C

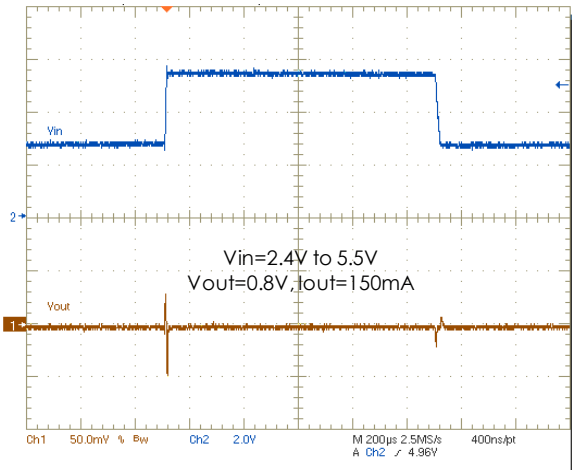
Enable Response (V_{OUT}=3.3V)



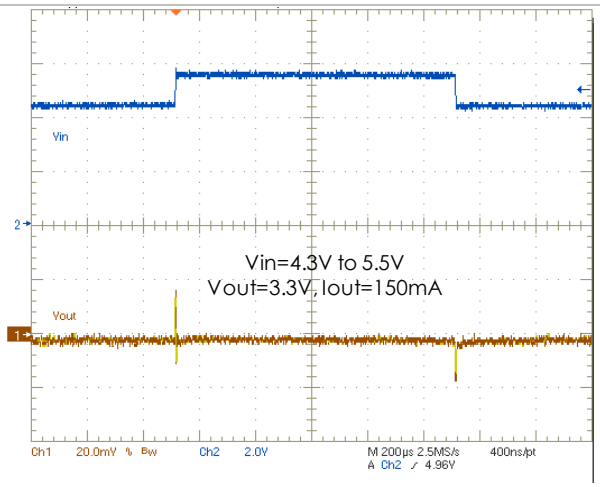
Disable Response (V_{OUT}=3.3V)



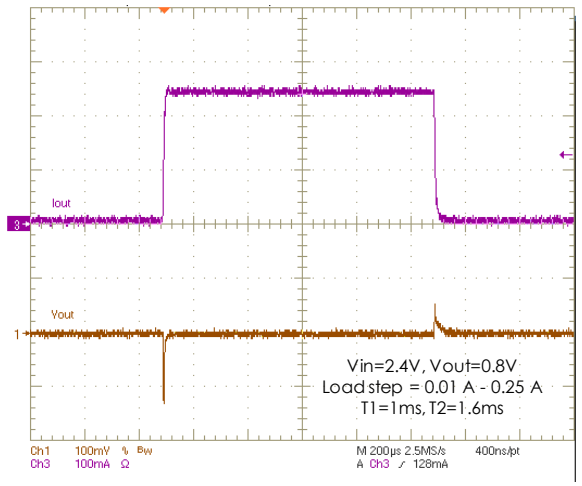
Line Transient (Vout=0.8V)



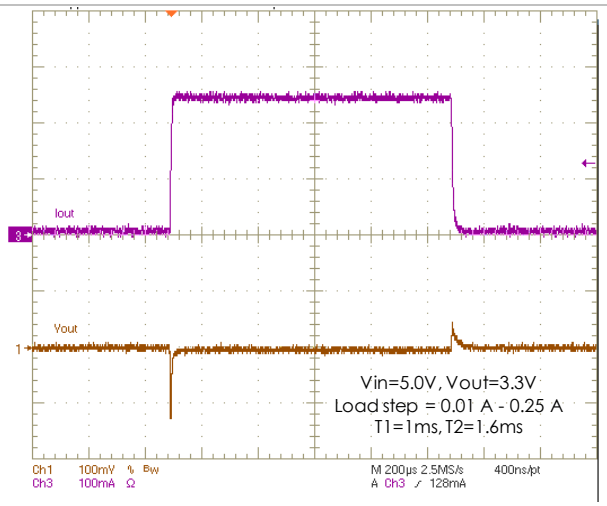
Line Transient (Vout=3.3V)



Load transient (V_{OUT}=0.8V)



Load transient (V_{OUT}=3.3V)



Application Information

General Description

Referring to Fig.1 as shown in the Functional Block Diagram section, the EMP8150 adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The sub Vout-select form the feedback circuit which samples the output voltage for the error amplifier's non-inverting input. The inverting input is set to the bandgap reference voltage. Due to its high open-loop gain, the error amplifier ensures that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset voltage reference voltage. The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor, which controls the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register these changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. The regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the temperature and current protection circuitry.

Output Capacitor

The EMP8150 is specially designed for use with ceramic output capacitors of as low as 1μF to take advantage of the savings in cost and space, as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the EMP8150 are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

No-Load Stability

The EMP8150 is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

Input Capacitor

A minimum input capacitance of 1μF is required for EMP8150. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

Power Dissipation

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$$T_J = \theta_{JA} \times (P_D) + T_A$$

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

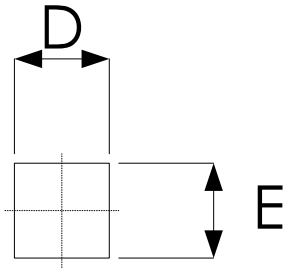
$$P_D = I_{OUT} (V_{IN} – V_{OUT})$$

As the above equations show, it is desirable to work with Ics whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermally overloading the EMP8150, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

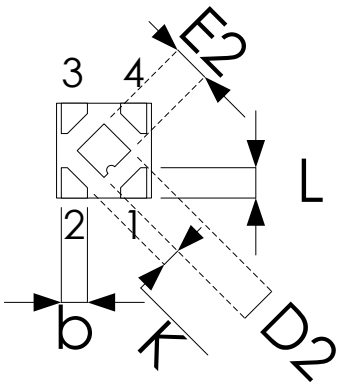
Shutdown

The EMP8150 enters shutdown mode when the EN pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically < 0.5uA. The low supply current makes the EMP8150 best suited for battery-powered applications. The maximum guaranteed voltage at the EN pin to enter shutdown mode is 0.4V. A minimum guaranteed voltage of 1.2V at the EN pin will activate the EMP8150. To constantly keep the regulator on, direct connection of the EN pin to the V_{IN} pin is allowed.

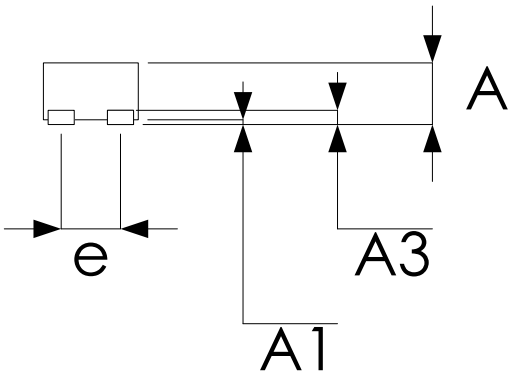
Package Outline Drawing
uDFN-4L (1mm x 1mm)



TOP VIEW



BOTTOM VIEW



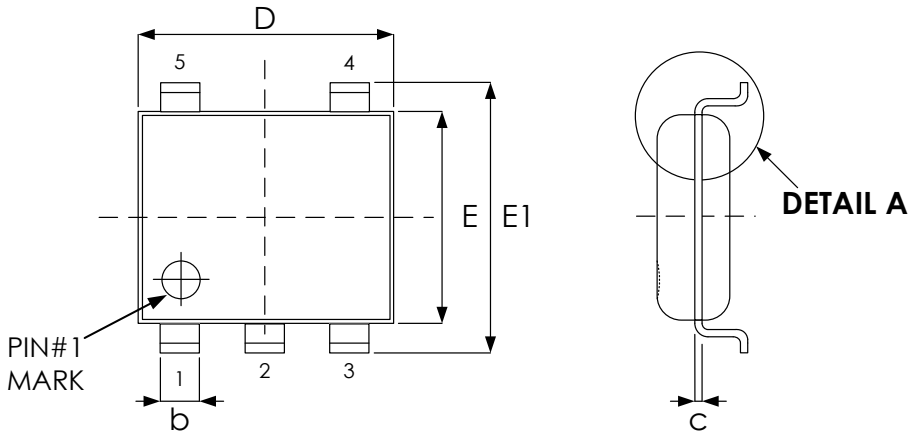
SIDE VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.35	0.60
A1	0.00	0.05
A3	0.12 REF.	
b	0.175	0.275
D	1.00 BSC	
E	1.00 BSC	
e	0.625 BSC	
L	0.200	0.300
K	0.20	-

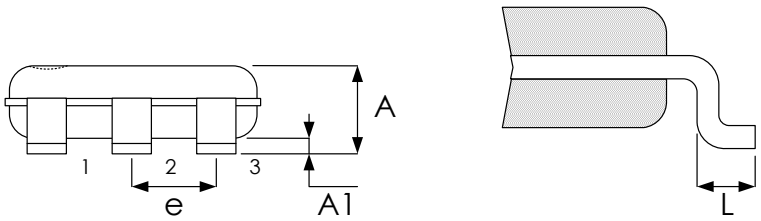
Exposed pad

	Dimension in mm	
	Min	Max
D2	0.40	0.60
E2	0.40	0.60

Package Outline Drawing
SOT-23-5



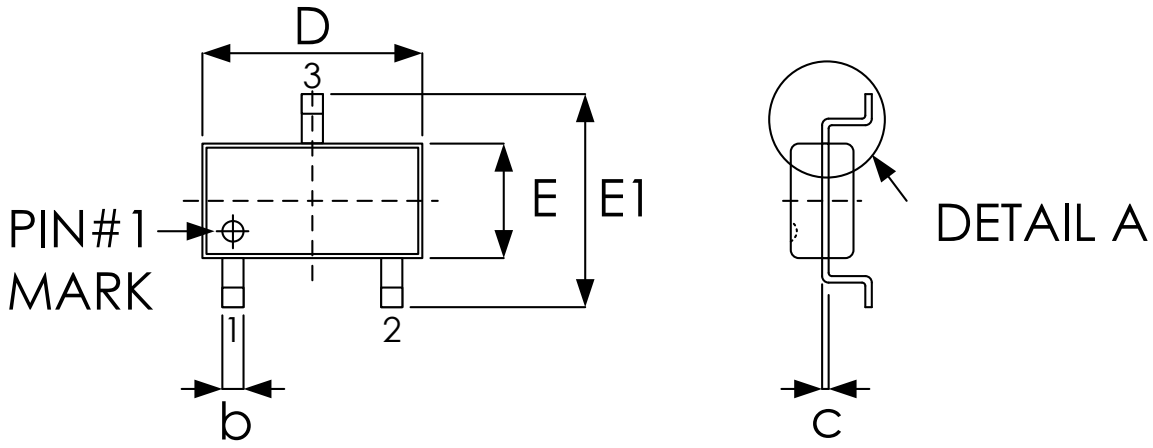
TOP VIEW



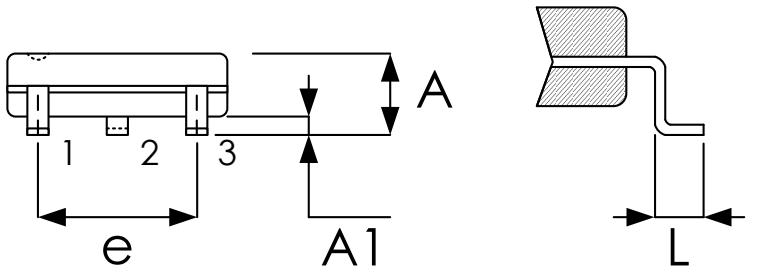
SIDE VIEW **DETAIL A**

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60

Package Outline Drawing
SOT-23-3



TOP VIEW



SIDE VIEW **DETAIL A**

Symbol	Dimension in mm	
	Min.	Max.
A	0.90	1.45
A1	0.00	0.15
b	0.30	0.50
c	0.08	0.25
D	2.70	3.10
E	1.40	1.80
E1	2.60	3.00
e	1.90 BSC	
L	0.30	0.60

Revision History

Revision	Date	Description
0.1	2018.09.18	Original
0.2	2018.10.17	Add SOT-23 3LDS package information
0.3	2018.11.27	Input voltage range and maximum output current modify
0.4	2019.02.20	Add new voltage option for SOT23-5 and uDFN
0.5	2019.05.29	Update POD for uDFN
0.6	2019.07.10	Modified Electrical Characteristics table VDO typical value and added MAX value.
0.7	2019.08.23	Add new voltage option for SOT23-3,SOT23-5 and uDFN
1.0	2020.05.12	Remove Preliminary word for RP
1.1	2020.07.03	Add Pin1 location description for UDFN

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